Swarup Bhunia, Ph.D.

T. and A. Schroeder Associate Professor

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Google Scholar: http://scholar.google.com/citations?user=JZ3awVAAAAAJ&hl=en

Research Interests

- ***Hardware Security and Trust***, *with emphasis on*: anti-counterfeiting, anti-Trojan, authentication, & anti-piracy solutions
- ***Adaptive Nanocomputing*** with emerging technologies
- ***Computing at Extreme***, *with emphasis on:* nanomechanical logic and memory
- ***Low-power and Robust Electronics***
- ***Bioimplantable and Wearable Systems***

Education

Ph.D. 2000-2005 **Purdue University, West Lafayette, USA**, Electrical and Computer Engineering
Thesis: "Power and Yield-Aware Design and Test of Nano-Scale CMOS Circuits"
Advisor: K. Roy
Dissertation Committee: K. Roy (chair), C.K. Koh, K. Muhammad, and T.N. Vijaykumar

M.Tech. 1995-1997 **Indian Institute of Technology, Kharagpur, India**, Computer Science
Title: "Design and Simulation of an ASIC for Fractal Image Compression"
Advisor: P.P. Das

B.E. 1991-1995 **Jadavpur University, Kolkata, India**, Computer Science

Professional Experience

July 2011-current
Associate Professor (Tenured)
Electrical Engineering and Computer Science
Case Western Reserve University, Cleveland, OH, USA

August 2005-June 2011
Assistant Professor (Tenure-track)
Electrical Engineering and Computer Science
Case Western Reserve University, Cleveland, OH, USA

May 2003-August 2003
Summer Intern
Intel Corporation
Austin, TX, USA

May 2002-August 2002
Summer Intern
Intel Corporation
Austin, TX, USA

Sept 1997-July 2000	**Senior Engineer** Interra Systems San Jose, CA, USA
Feb 1997-Aug 1997	**Senior Engineer** Sasken Communication Technologies Limited [formerly, Silicon Automation Systems, Inc. (SAS)] Bangalore, India

Honors and Awards

2013	Excellence in Research Award, EECS, Case Western Reserve University
2013	IBM Faculty Award
2013	Appointment for T. and A. Schroeder Chair Professorship in Computer Science and Engineering
2012	Best paper award, 25th International Conference on VLSI Design
2011	National Science Foundation (NSF) career development (CAREER) award
2011	Mike Mesarovic award for extraordinary impact, EECS, Case Western Reserve University
2010	Best paper candidate, IEEE Hardware Oriented Security and Trust Symposium (HOST)
2009	Semiconductor Research Corporation (SRC) Inventor Recognition Award
2006	Best paper nomination in Asia and South Pacific Design Automation Conf. (ASP-DAC)
2005	Semiconductor Research Corporation (SRC) Technical Excellence award (as team member)
2005	E.J. McCluskey Best Doctoral Thesis Award by Test Tech. Technical Council (TTTC), 3rd place
2004	Best paper award in International Conference on Computer Design (ICCD)
2003	Best paper award in Latin American Test Workshop (LATW)

Professional Memberships

Senior Member of Institute of Electrical and Electronic Engineers (IEEE)	*2009-present*
Faculty Member and Advisor of *Eta Kappa Nu* (*HKN*)	*2010-present*
Investigator of Advanced Platform Technology (APT) Center in Cleveland, OH	*2013-present*

Research Grant and Contract Support

Current

10/2014-09/2017	"SaTC:STARSS: IPTrust: A Comprehensive Framework for IP Integrity Validation" Source: **NSF** (Award #: CNS-1441705) Role: **Principal Investigator** Other Participants: PI of Collaborative Project: P. Mishra (UFL)
12/2014-11/2015	"Malleable Memory-Centric Hardware Accelerator Using RRAM for Data-Intensive Applications: Device-Circuit-System Co-Design Approach" Source: **Semiconductor Research Corporation (SRC)** Role: **Principal Investigator** Other Participants: None
02/2014-01/2017	"Infrastructure IP for Security: A Scalable Solution to Secure SoC" Source: **Semiconductor Research Corporation (SRC)** Role: **Principal Investigator** Other Participants: None

9/2013-08/2015 "TUES:Type1:Collaborative: An Integrative Hands-on Approach to Security Education for Undergraduate Students"
Source: **NSF** (Award #: DUE- 1245756)
Role: **Principal Investigator**
Other Participants: PIs of Collaborative Project: S. Mal-Sarkar, Co-PI: C. Yu (CSU)

6/2011-08/2016 "CAREER: An Integrative and Scalable Approach to Embedded Hardware Protection"
Source: **NSF** (Award #: CNS-1054744)
Role: **Principal Investigator**
Other Participants: None

9/2011-08/2015 "SHF:Small: Device-Circuit-Architecture Co-Design for Reconfigurable Computing at the Extreme"
Source: **NSF** (Award #: CNS-1054744)
Role: **Principal Investigator**
Other Participants: Co-PI: M. Mehregany (CWRU), P. Feng (CWRU)

9/2013-08/2015 IBM Faculty Award on Coprocessor for Data Analytics Kernels
Source: **IBM**
Role: **Principal Investigator**
Other Participants: None

4/2012-03/2016 "Wireless Implantable Pressure Monitor for Improved Neuromodulation"
Source: **U.S. Department of Veterans Affairs (VA)**
Role: **Co-Investigator**
Other Participants: PI: M. Damaser (CCF), Co-Is: K. Gustavson (CWRU), W. Ko (CWRU), and others

Completed

07/2010-6/2014 "Collaborative Research: Reconfigurable Computing Using 2D Nanoscale Memory for Multimedia Signal Processing"
Source: **NSF** (Award #: ECCS-1002237)
Role: **Principal Investigator**
Other Participants: PI of Collaborative Project: S. Mukhopadhyay (GaTech)

09/2010-9/2014 "SHF: Medium: Collaborative Research: System Level Self Correction Using On-Chip Micro Sensor Network and Autonomous Feedback Control"
Source: **NSF** (Award #: CCF-0964514)
Role: **Principal Investigator**
Other Participants: PI of Collaborative Project: B. Jung (Purdue U.), Co-PI: K. Roy (Purdue U.)

04/2011-3/2013 "Techniques for Validation and Integrity of Soft IP Cores"
Source: **DARPA**
Role: **Co-Principal Investigator**
Other Participants: PI: C. Papachristou (CWRU), Co-PI: S. Clay (Rockwell)

02/2011-1/2012 "Width-Aware Dynamic Supply Gating for Low Power Datapath & Memory"
Source: **Intel Corporation**
Role: **Principal Investigator**
Other Participants: None

08/2011-07/2012	"Electromechanical Computing at High Temperature Using Poly-SiC NEMS" Source: **DARPA** Role: **Co-Principal Investigator** Other Participants: PI: M. Mehregany (CWRU), Co-PI: P. Feng (CWRU)
08/2008-7/2011	"Batch-Fabricated Nanochannel Devices for Direct Electrical Probing of Biomolecules" Source: **NSF** (Award #: ECCS-0924808) Role: **Co-Principal Investigator** Other Participants: PI: C. Mastrangelo (U. of Utah)
06/2008-5/2011	"Fine-Grain Power Management & Monitoring Circuits" Source: **Intel Corporation** Role: **Principal Investigator** Other Participants: None
01/2009-12/2010	"High-Temperature Logic Using Poly-SiC NEMS" Source: **DARPA** Total Amount: **$529,960** Role: **Co-Principal Investigator** Other Participants: PI: M. Mehregany (CWRU)
05/2008-4/2009	"Minimally Invasive Multi-Parameter Side-Channel Approach for Sequential Trojan Detection" Source: **DARPA** Role: **Principal Investigator** Other Participants: Co-PI: C. Papachristou (CWRU), Co-PI: K. Roy (Purdue U.)
04/2007-3/2008	"Standby Leakage Reduction and Data Retention Using Hybridization with SiC NEMS Switches" Source: **DARPA** Role: **Co-Principal Investigator** Other Participants: PI: M. Mehregany (CWRU)

Small Equipment Grants

04/2007	FPGA Development Boards + Quartus Software Suite Source: **Altera Corporation**
05/2008	Two high-performance desktop computers Source: **Intel Corporation**
04/2007 & 01/2014	FPGA Development Boards + ISE Software Suite Source: **Xilinx Corporation**

Student Supervising Activities

PhD Students

07/2014 Yu Zheng (*currently at* LSI Corporation, San Jose, USA)

03/2014	Steve Majerus	(*currently at* US Dept. of Veteran Affairs, Cleveland, USA) [Acting Advisor]
08/2013	Xinmu Wang	(*currently at* Qualcomm Inc., San Diego, USA)
04/2012	Seetharam Narasimhan	(*currently at* Intel Corporation, Portland, USA)
07/2011	Somnath Paul	(*currently at* Intel Corporation, Portland, USA)
06/2010	Rajat Subhra Chakraborty	(*currently tenured faculty at* Indian Institute of Tech., Kharagpur, India)
07/2015*	Abhishek Basak	(*In progress, PhD Candidate*)
12/2015*	Wenchao Qian	(*In progress, PhD Candidate*)
06/2016*	Robert Karam	(*In progress, PhD Candidate*)
06/2017*	Fengchao Zhang	(*In progress, PhD Candidate*)
05/2018*	Kai Yang	(*In progress, PhD Candidate*)

**Expected graduation date*

MS Students

06/2013	Vaishnavi N. Ranganathan	(*with thesis*)
06/2013	MaryamSadat Hashemian	(*with thesis*)
03/2013	Anandaroop Ghosh	(*with thesis*)
06/2012	Lei Wang	(*with thesis*)
04/2012	E-Jen Lien	(*with thesis*)
03/2011	Keerthi Kunaparaju	(*with thesis*)
06/2010	Dongdong Du	(*with thesis*)
03/2010	David Stalter	(*with thesis*)
06/2007	Lawrence Lienweber	(*with thesis*)
12/2007	Yu Zhou	(*with thesis*)
12/2007	Matthew Holtz	(*with project*)
05/2015*	Christopher Babecki	(In progress, MS Candidate)
08/2015*	Andrew Hennessy	(In progress, MS Candidate)
08/2016*	Sean Vora	(In progress, MS Candidate)

**Expected graduation date*

Research Experience for Undergraduates

Summer, Fall 2014	Tom Shkurti
Summer, Fall 2014	Rebecca Frederick
Summer 2014	Kei Hitomi
Summer 2014	Tina Alam, Arizona State University
Fall 2013, Spring 2014	Luke Gould
Spring 2014	Jean Castillo
Spring 2014, Summer 2014	Andrew Hennessy
Fall 2013, Spring 2014	Christopher Babecki
Fall 2012	Christian Gunderman
Summer 2011, Fall 2011	Shawn Halpin
Fall 2010	Brian Widman
Fall 2010	Margaret Robson

Senior Projects

Fall 2015	Steve Paley
Spring 2014	Matt McKee, Brian Hayt, Kenneth Akiki, Rachid Lamouri, Casey Stoessl
Spring 2014	Luke Gould
Fall 2013	Andrew Pentz, John Clark, Nicholas Wietecha
Spring 2013	Patrick Landis and Schuyler Thomson
Spring 2013	Timothy March and Linneker Carvajal

Spring 2011	Margaret Robson, Stephanie Diehl, Ben Applequist, Philip Miller
Spring 2010	Steve Knab, Justin Michel, Michael Slattery
Summer 2009	Thomas Ramps
Spring 2009	Russel Smith, Nidhi Garg, Ermal Dreshaj, Brad Collins
Fall 2008	Alex Cassidy

High-School Students

Summer 2010 – Spring 2013 Tatini Mal-Sarkar (*currently* a "Rabi Scholar" at Columbia University, USA)

Award to Student Advisees

Graduate students Abhishek Basak, Fengchao Zhang, and Vida Pashaei selected for participation in the final round of competition, in *Embedded Systems Challenge (ESC) in NYU-Poly Cyber Security Awareness Week*, 2014

Team of graduate students (Andrew Hennessey, Fengchao Zhang, and Yu Zheng) enter into the final round of *CSI CyberSEED week Hardware Challenge*, U. of Connecticut (UCONN), 2014

Graduate student Abhishek Basak and Vaishnavi Ranganathan win the **Student Paper Competition (second place)** in *IEEE EMBS Special Topic Conference on Point-of-Care Healthcare Tech. (PoCHT)*, 2013

Undergraduate students Patrick Landis and Schuyler Thomson are awarded the **Best Senior Project** in the department of EECS, Spring 2013

Graduate students Yu Zheng and Abhishek Basak receives **honorable mention** in the final round of competition, in *Embedded Systems Challenge (ESC) in NYU-Poly Cyber Security Awareness Week*, 2013

Graduate student Somnath Paul receives the **EDAA Outstanding Dissertation Award** from the *European Design Automation Association*, 2012

High School student Tatini Mal-Sarkar wins the **Student Paper Award** (Sponsored by Intel Corporation) in *25th IEEE Intl. Symp. on Defect and Fault Tolerance in VLSI & Nanotechnology Systems (DFTS)*, 2012

Graduate student Abhishek Basak is selected **Student Paper Competition (SPC) Finalist** in *34th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, 2012

Graduate student Somnath Paul earns the **Ruth Barber Moon award**, from the *Case School of Graduate Studies* for excellence in academic promise and leadership quality, 2011

Graduate students Xinmu Wang, Aswin Krishna, and Seetharam Narasimhan win the **Third Prize in the NYU-Poly CSAW Hardware Trojan Design Challenge** [7th Annual CSAW Challenge], 2010

Graduate student Rajat Subhra Chakraborty selected **semi-finalist** in the **TTTC E. J. McCluskey Best Doctoral Thesis Award contest**, held at the *IEEE VLSI Test Symposium (VTS)*, 2010

Graduate student Somnath Paul thesis topic selected **semi-finalist** in **ACM Student Research Competition** at *47th Design Automation Conference (DAC)*, 2010

Graduate student Seetharam Narasimhan selected as **Student Paper Competition (SPC) Finalist** in the *IEEE Engineering in Medicine and Biology Society (EMBS)* Student Paper Competition, 2009

Graduate student Rajat Subhra Chakraborty earns the **Ruth Barber Moon award**, from the *Case School of Graduate Studies* for excellence in academic promise and leadership quality, 2009

Graduate student Seetharam Narasimhan earns the **Ruth Barber Moon award**, from the Case School of Graduate Studies for excellence in academic promise and leadership quality, 2008

Teaching Activities

Associate Professor, EECS Department, Case Western Reserve University (CWRU)

Semester	Course	Enrollment	Contact Hours	Teaching Assistants
Sp. 2015	**Computer Architecture** (*EECS 314*)	111	3	3
Fall 2014	**Hardware Security** *(EECS 397)* A new hands-on course targeted to the sophomore and junior-level undergraduate students on fundamentals of electronic hardware security issues and countermeasures for all Engineering majors.	12	3	
Sp. 2014	**Computer Architecture** (*EECS 314*) An undergraduate course on processor architecture, hardware-software interface and low-level programming. Includes a design project.	81	3	2
Fall 2013	**Volts, Amps, Bits, Bytes** *(FSNA 137)* A SAGES first seminar course for freshman students on fundamental working principles of electronics/computers. Includes a series of lab assignments, a final design project, and 4-6 site visits in the 4th hour.	17	4	0.5
Fall 2013	**Nanometer VLSI Design** *(EECS 495)*	3	3	0
Sp. 2013	**Computer Architecture** (*EECS 314*)	62	3	2
Fall 2012	**Volts, Amps, Bits, Bytes** *(FSNA 137)*	19	4	0.5
Sp. 2012	**Computer Architecture** (*EECS 314*)	56	3	2
Sp. 2012	**Hardware Security** *(EECS*	7	3	0
Fall 2011	**Nanometer VLSI Design** *(EECS 495)*	2	3	0

Assistant Professor, EECS Department, Case Western Reserve University (CWRU)

Semester	Course	Enrollment	Contact Hours	Teaching Assistants
Sp. 2011	**Hardware Security** *(EECS 397)*	8	3	0
Sp. 2011	**Computer Architecture** (*EECS 314*)	75	3	2
Fall 2010	**Nanometer VLSI Design** *(EECS 495)*	11	3	0
Sp. 2010	**Computer Architecture** (*EECS 314*)	52	3	2
Fall 2009	**Nanometer VLSI Design** *(EECS 495)*	8	3	0
Fall 2009	**Digital Logic Laboratory** (*EECS 301*) A laboratory course on digital system design using FPGA boards. Jointly instructed with Ed Burwell.	16	2	1
Sp. 2009	**Computer Architecture** (*EECS 314*)	75	3	2

Fall 2008	**Nanometer VLSI Design** *(EECS 495)*	16	3	0
Fall 2008	**Digital Logic Laboratory** (*EECS 301*)	8	2	1
Sp. 2008	**Computer Architecture** (*EECS 314*)	66	3	2
Fall 2007	**Nanometer VLSI Design** *(EECS 495)*	8	3	0
Sp. 2007	**Computer Architecture** (*EECS 314*)	70	3	2
Fall 2006	**Nanometer VLSI Design** *(EECS 495)*	6	3	0
Sp. 2006	**Computer Architecture** (*EECS 314*)	68	3	2
Fall 2005	**Nanometer VLSI Design** *(EECS 495)*	2	3	0

Professional Leadership and Service Activities

Editorial Activities

Associate Editor (AE) for the *IEEE Transactions on Multi-Scale Computing Systems (TMSCS)* — *2015-2016*

Associate Editor (AE) for the *IEEE Trans. on Computer-Aided Design of Integrated Circuits Systems (TCAD)* — *2014-present*

Associate Editor (AE) for *ACM Journal on Emerging Technologies in Computing Systems* — *2010-present*

Associate Editor (AE) for the *Journal of Low Power Electronics (JOLPE)* — *2009-present*

Guest Editor (GE) for *Transactions on Multi-Scale Computing Systems (TMSCS) Special Issue on "Wearables, Implants, and Internet of Things"* — *Dec 2015*

Guest Editor (GE) for *IEEE Journal of Emerging and Selected Topics in Circuits and Systems (JETCAS) Special Issue on "Computing in Emerging Technologies (Second Issue)"* — *March 2015*

Guest Editor (GE) for *IEEE Journal of Emerging and Selected Topics in Circuits and Systems (JETCAS) Special Issue on "Computing in Emerging Technologies (First Issue)"* — *Dec 2014*

Guest Editor (GE) for *IEEE Design & Test of Computers (D&T) Special Issue on "Trusted Design with Untrusted Components"* — *March 2013*

Guest Editor (GE) for *ACM Journal on Emerging Technologies in Computing Systems (JETC) Special Issue on "Implantable Electronics"* — *June 2012*

Guest Editor (GE) for *Journal of Low Power Electronics (JOLPE) Special Issue on "Low-Power Track papers in International Conference of VLSI Design"* — *Oct 2010*

Guest Editor (GE) for *IEEE Design & Test of Computers (D&T) Special Issue on "Post-Silicon Calibration and Repair"* — *Nov 2010*

Conference Organizing Committee Memberships

Publicity Chair, 29th International Conference on VLSI Design (VLSI Design) — *2016*

Publicity Chair, 4th Intl. Conf. on Security, Privacy and Applied Cryptography Eng. (SPACE) — *2015*

Program Chair, 8th IEEE Int. Symposium on Hardware-Oriented Security and Trust (HOST) — *2015*

North-America Liaison for the 16th IEEE Latin American Test Workshop (LATW) — *2014*

Publicity Chair, 3rd Intl. Conf. on Security, Privacy and Applied Cryptography Eng. (SPACE) — *2014*

Program Chair, 18th International Symposium on VLSI Design and Test (VDAT) — *2014*

Publicity Chair, 7th IEEE Intl. Symposium on Hardware Oriented Security and Trust (HOST) — *2014*

Program Chair, 9th IEEE/ACM Intl. Symposium of Nanoscale Architectures (NANOARCH) — *2013*

Publicity Chair, 6th IEEE Intl. Symposium on Hardware Oriented Security and Trust (HOST) *2013*

Publicity Chair, 2nd Intl. Conf. on Security, Privacy and Applied Cryptography Eng. (SPACE) *2012*

Program Chair, 17th IEEE Intl. Mixed-Signals, Sensors, and Systems Test Workshop (IMS3TW) *2011*

Publication Chair, 11th IEEE International On-Line Testing Symposium (IOLTS), 2005 *2005*

Workshop and Session Organization

Organizer and Moderator of Panel on *Beyond-CMOS computing*, *IEEE VLSI Design and Test Symposium (VDAT)* *2014*

Organizer of Panel *on Future of Nanoelectronics*, *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)* *2013*

Co-organizer and Moderator, Hot Topic Session on *Hardware Security*, at the *IEEE VLSI Test Symposium (VTS)* *2010*

Subcommittee/Track Chair of Technical Program Committee

Track Chair for Prototyping, Verification, Modeling, and Simulation, 23rd IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) *2015*

Track Chair of Security and Fault-Tolerant Systems Track, 20th Asia and South Pacific Design Automation Conference (ASP-DAC) *2015*

Track Chair of Digital Design Track, 27th International Conference on VLSI Design (VLSI Design) *2014*

Track Chair for Track T6-Devices, Circuits and Systems for Emerging Technologies, 21st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) *2013*

Track Chair of Low Power Track, 24th International Conference on VLSI Design (VLSI Design) *2011*

Track Chair of Low Power Track, 23rd International Conference on VLSI Design (VLSI Design) *2010*

Technical Program Committee Membership

52nd Design Automation Conference (DAC) *2015*

16th International Symposium on Quality Electronic Design (ISQED) *2015*

28th International Conference on VLSI Design (VLSI Design) *2015*

10th ACM/IEEE International Symposium on Nanoscale Architectures (NANOARCH) *2014*

22nd IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) *2014*

15th International Symposium on Quality Electronic Design (ISQED) *2014*

4th International Conference on Security, Privacy, and Applied Cryptography Eng (SPACE) *2014*

7th IEEE International Symposium on Hardware-Oriented Security and Trust (HOST) *2014*

51st Design Automation Conference (DAC) *2014*

15th International Symposium on Quality Electronic Design (ISQED) *2014*

3rd International Conference on Security, Privacy, and Applied Cryptography Eng (SPACE) *2013*

5th IEEE International Symposium on Hardware-Oriented Security and Trust (HOST) *2013*

International Conference on VLSI Design (VLSI Design) *2012-2013*

18th IEEE International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW) *2012*

4th IEEE International Symposium on Hardware-Oriented Security and Trust (HOST) *2012*

Workshop on Cryptographic Hardware and Embedded Systems (CHES) *2011-2012*

IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH) *2007-2011*

International Conference on Security Aspects in Information Technology, High-Performance Computing and Networking (InfoSecHiComNet) *2011*

Design Automation and Test in Europe (DATE), 2011 *2006-2011*

IEEE International Symposium on VLSI (ISVLSI), 2011 *2008-2011*

20th IEEE Asian Test Symposium (ATS) *2011*

IEEE International Symposium on Low Power Electronics and Design (ISLPED) *2007-2010*

IEEE/ACM Nanoscale Architecture Symposium (NANOARCH) *2007-2010*

IEEE Hardware Oriented Security and Test (HOST) Symposium	*2008-2010*
Test Technology Educational Program (TTEP) by IEEE Computer Society	*2006-2009*
IFIP/IEEE International Conference on VLSI (VLSI-SoC)	*2008*

Session Chair

56th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)	*2013*
Keynote session in the 9th IEEE/ACM International Symposium on Nanoscale Architectures	*2013*
IEEE Symposium on Hardware Oriented Security and Trust (HOST)	*2013*
International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)	*2012*
IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)	*2010*
IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)	*2010*
International conference on VLSI Design (VLSI Design)	*2010*
IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)	*2008*
IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)	*2008*
International Symposium on Low Power Electronics and Design (ISLPED)	*2007*
IEEE International Conference on Computer Aided Design (ICCAD)	*2007*

Review Activities

Reviewer for the *IEEE Trans. VLSI Systems (TVLSI), IEEE Trans. on CAD (TCAD), IEEE Trans. on Computers (TComp), IEEE Trans. on Circuits and Systems (TCAS), Journal of Electronic Testing: Theory and Applications (JETTA), ACM Trans. on Design Automation of Electronic System (TODAES), IEEE Design & Test of Computers, ACM Journal of Emerging Tech. and Comp. (JETC), IEEE Embedded Systems Letter (ESL), IEEE Transactions on Information Forensics and Security (TIFS), IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), IEEE Electron Device Letters (EDL), IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), Journal of Neural Engineering (JNE), IEEE Transactions on Reliability (TR), and Journal of Microscopy*

Other Services

SAGES course syllabus included in Online Ethic Center for the National Academy of Eng.	*2014*
Contributed an one-page article in SIGDA E-Newsletter (December)	*2014*
Created a Social Networking Group in Facebook on *Hardware Security w/ over 300 members*	*2010*
Created Wiki pages on reconfigurable computing with memory & hardware obfuscation	*2010 (x2)*
Contribution of lecture materials to Synopsys University Program on low-power design	*2008*

University Administrative Leadership and Service Activities

University

University Undergraduate Faculty (UUF) Academic Standing Committee	*2009-2010*
Research Showcase Judge	*2007-2014*

Case School of Engineering

EECS Chair Search Committee	*2013*
Research Committee	*2009-2010*

Department

ABET Academic Representative for Computer Engineering	*2011-present*
Computer Engineering Program Undergraduate Advisor	*2010-present*
Computer Engineering Program Representative	*2011-present*

Meeting with alumnus and prospective students	*2010-present*
CE Faculty Search Committee Member	*2014*
Mentoring committee member for Philip Feng, Ming-Chun Huang	*2014*
Freshmen Advisor	*2012-2013*
CE Qualifier Exam (Assistance with setting exam and evaluation)	*2008-2013*
Host and organizer for distinguished speaker series seminars	*2011-2012*
Choices Fair Computer Engineering Representative	*2012*
EECS Curriculum and Accreditation Committee Member	*2007-2009*
Organizer of Departmental Town-Hall Meeting	2006
EECS Curriculum and Accreditation Committee Member	*2005*

Dissertation and Exam Committee Service Activities

PhD Dissertation Committee Service (excluding my students)

Ting He (EE)	*2015*
Bobby Lu (EE)	*2014*
Bardia Bozorgzadeh (EE)	*2014*
Kanokwan (Nok) Limnuson (EE)	*2014*
Chia-Wei Soong (EE), Steve Majerus (EE)	*2013 (x2)*
Zheng Liu (CS)	*2011*
Te-Hao Lee (EE)	*2009*
Huthaifa Al-Omari (CE), Hyun Kim (CS)	*2008 (x2)*
Jung Hwan Choi (ECE, Purdue U.)	*2007*
Jen-Chieh Ou (CE)	*2006*

MS Thesis Committee Service (excluding my students)

Tyler Goeringer, Achiranshu Garg (NTU, Singapore)	*2012 (x2)*
Prapan Shewinvanakitkul	*2011*
Ming-Hsuan Hsu, Nitin Reddy, David Tian, Patrick Rawlinson (EECS, CWRU)	*2009 (x3)*
Shruthi Rnganathan, Zemeng Li, Ying Ying Wang	*2008 (x3)*
Manjulatha Kamalraj, David Young, Prasanna V. Govindarajan	*2007 (x3)*
Moiz Neemuchwala, Sivasubramaniam Krishnamurthy, Pranay Nigam	*2006 (x3)*

PhD Oral Qualifying Exam Committee

Srihari Rajgopal	*2014*
Chia-Hua "Charlie" Lin	*2010*
Noppasit Laotaveerungrueng	*2006*

Entrepreneurial Activities

Sept 2014 **Co-founder and Chief Technology Officer** of startup ***HakHam Systems, LLC*** along with two CWRU students (Andrew Hennessy and Jonathan Hall) on hardware ecosystem for cybersecurity education and training. Website: http://www.hakhamsystems.com/

Aug 2014 **Academic collaborator** in a startup ***TruSecSys*** on Hardware based security and trust. The company targets marketing some of the security primitives (patented by CWRU) developed by Dr. Bhunia's group. Website: http://www.trusecsys.com/

Media Coverage

Oct. 2014 Undergraduate security course on hardware hacking in the THINK Magazine and Case School of Engineering Annual Report.

Sept. 2014 National Science Foundation (NSF) & Semiconductor Research Corporation (SRC) STARSS grant to develop Secure and trustworthy Systems. [EETimes] [NSF] [SRC]

Aug. 2014 Hacking based security curriculum for undergraduate students. [National Public Radio (NPR) Marketplace]

March 2014 Comprehensive security curriculum development for Undergraduate, a joint effort with Cleveland State University [The Plain Dealer] [Physorg] [WTAM Radio]

Dec. 2013 Collaborative research on nanoscale energy-efficient mechanical devices. [THINK] [ScienceDaily] [Physorg]

Oct. 2013 Research on cancer detecting wearable vest with integrated ultrasound transducers. [THINK] [Case Daily] [MedicalExpress]

Oct. 2012 Research on energy-efficient computing is featured in Case School of Engineering Annual Report. [Link]

March 2012 Research on low power processor using advanced power gating. [ScienceDaily] [Physorg] [eScienceNews] [ScienceCodex] [newswise] [ScienceNewsOnline] [energyDaily]

Oct. 2011 Research on extreme environment computing is featured in Case School of Engineering Annual Report. [Link]

Oct. 2010 Collaborative research on electromechanical computing for harsh environment. [ScienceDaily] [Physorg] [nanowerk] [NewScientist] [PhysicsWorld] [Slashdot]

Oct. 2010 Collaborative research on electromechanical computing is reviewed in *the "Research Highlights"* section of *Nature Nanotechnology*.

Publications (Chronological Order)

Publications are listed in chronological order. Names of student co-authors whose research Dr. Bhunia has supervised, including visiting students, are underlined.
On-line copies of most publications can be found at: http://engr.case.edu/bhunia_swarup/publication.html

Journal Publications *(Refereed)*

1. **Swarup Bhunia**, Michael Hsiao, Mainak Banga, and Seetharam Narasimhan, "Hardware Trojan Attacks: Threat Analysis and Countermeasures", *Proceedings of the IEEE (PIEEE)*, vol. 102, no. 8, pp. 1229-1247, 2014.
2. Sandip Ray, Jongsun Park, and **Swarup Bhunia**, "Wearables, Implants, and Internet of Things: Towards Unifying Technologies to Support Diverse Paradigms", to appear in IEEE *Transactions on Multi-Scale Computing Systems (TMSCS)*. [Perspective paper in the Special issue on Wearables, Implants, and Internet of Things].
3. Wen Yueh, Subho Chatterjee, Muneeb Zia, Student Member, **Swarup Bhunia**, and Saibal Mukhopadhyay, "A Memory-Based Logic Block with Optimized-for-Read SRAM for Energy-efficient Reconfigurable Computing Fabric", to appear in *IEEE Transactions on Circuits and Systems II (TCAS-II)*.
4. Deliang Fan, **Swarup Bhunia**, Saibal Mukhopadhyay, and Kaushik Roy, "Exploring Spin Transfer Torque Devices for Unconventional Computing", to appear in IEEE *Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*. [Perspective paper in the Special issue on Computing in Emerging Technologies].
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10. Jongsun Park, Jangwon Park and **Swarup Bhunia**, "VL-ECC: Variable Data-Length Error Correction Code for Embedded Memory in DSP Applications", *IEEE Transactions on Circuits and Systems II (TCAS-II), 2014*. VOL. 61, NO. 2, FEBRUARY 2014, pp. 120-124. doi: 10.1109/TCSII.2013.2291091
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Conference Publications *(Full-Paper Refereed Archival Conferences)*

1. Jae-Won Jang, Jongsun Park, Swaroop Ghosh, and **Swarup Bhunia**, "Self-Correcting STTRAM under Magnetic Field Attacks", to appear in *Design Automation Conference (DAC)*, 2015.
2. Andrew Hennessy, Fengchao Zhang, and **Swarup Bhunia**, "Trace Impedance based Authentication: A method towards Robust Counterfeit Printed Circuit Board (PCB) Detection", to appear in *33rd IEEE VLSI Test Symposium (VTS)*, 2015.
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15. **Swarup Bhunia** and Kaushik Roy, "Low Power Design under Parameter Variations", *International Symposium on Low Power Electronics and Design (ISLPED)*, 2008. [One page article on embedded tutorial] DOI: 10.1109/SOCC.2008.4641552
16. **Swarup Bhunia** and Kaushik Roy, "Power Dissipation, Variations and Nanoscale CMOS Design: Test Challenges and Self-Calibration/Self-Repair Solutions", *International Test Conference* (*ITC)*, pp. 1-10, 2007. [Lecture series article] DOI: 10.1109/TEST.2007.4437659

17. **Swarup Bhunia**, Saibal Mukhopadhyay, and Kaushik Roy, "Process Variations and Process-Tolerant Design", *International Conference on VLSI Design*, pp. 699-704, 2007. DOI: 10.1109/VLSID.2007.131

Book, Book Chapters and Editorials

Books

1. **Swarup Bhunia**, Steve Majerus, and Mohamad Sawan (Eds.), "Bioimplantable Systems: Design Principles and Applications", Elsevier, MA, USA, to be published in December 2014.
2. **Swarup Bhunia**, Sandip Ray, and Susmita Sur-Kolay (Eds.), "Fundamentals of IP and SoC Security: Design, Verification and Debug", to be published by Springer, New York, USA in May 2015.
3. Somnath Paul and **Swarup Bhunia**, "Computing with Memory for Energy-Efficient Robust Systems", Springer, New York, USA, August 2013.
4. **Swarup Bhunia** and Saibal Mukhopadhyay (Eds.), "Low-Power Variation-Tolerant Design in Nanometer Silicon", Springer, New York, USA, 1st Edition, ISBN: 978-1-4419-7417-4, November 2010.

Book Chapters

1. Rajat Subhra Chakraborty, Yu Zheng, and **Swarup Bhunia**, "Obfuscation-based SoC Design for Security against Piracy and Trojan Attacks", in "Secure System Design and Trustable Computing", edited by Chang Chip Hong and Miodrag Potkonjak, Springer International Publishing AG, Gewerbestrasse 11, 6330 Cham, Switzerland, to be published in August 2014.
2. Abhishek Basak and **Swarup Bhunia**, "Implantable Imager for Online Monitoring of Internal Organs", in Bioimplantable Systems: Design Principles and Applications", edited by Swarup Bhunia, Steve Majerus, and Mohamad Sawan, Elsevier, MA, USA, to be published in February 2015.
3. Sandip Ray, **Swarup Bhunia**, and Prabhat Mishra, "Security Validation in System-on-Chip", in Fundamentals of IP and SoC Security: Design, Verification, and Debug", edited by Swarup Bhunia, Sandip Ray, and Susmita Sur-Kolay, Springer, NY, USA, to be published in April 2015.
4. Abhishek Basak, Vaishnavi Ranganathan, Seetharam Narasimhan, and **Swarup Bhunia**, "Neural pattern recognition for closed-loop neuro-prosthesis", in "Implantable Bioelectronics - Devices, Materials and Applications", edited by Evgeny Katz, Wiley-VCH, August 2013.
5. **Swarup Bhunia** and Seetharam Narasimhan, "Hardware Trojan Detection", in "Introduction to Hardware Security and Trust", edited by Mohammad Tehranipoor and Cliff Wang, Springer, New York, USA, September 2011, ISBN: 978-1441980793.
6. **Swarup Bhunia** and Seetharam Narasimhan, "Ultralow Power Implantable Electronics", in "Handbook of Energy-Aware and Green Computing", edited by Sanjay Ranka and Ishfaq Ahmad, Chapman & Hall/CRC Press, January 2012, ISBN: 978-1439850404.
7. **Swarup Bhunia** and Kaushik Roy, "Low Power Design Techniques and Test Implications", in "Power-Aware Testing and Test Strategies for Low Power Devices", edited by Patrick Girard, Nicola Nicolici, and Xiaoqing Wen, Springer, New York, USA, 1st Edition, ISBN: 978-1441909275, August 2009. [Best-seller in *International Test Conference* 2009].

Editorials

1. Saibal Mukhopadhyay, Kaushik Roy, Hillery Hunter, and **Swarup Bhunia**, "Guest Editorial: Computing in Emerging Technologies (Second Issue)", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, March 2015.
2. **Swarup Bhunia,** Steve Majerus and Mohamad Sawan, "Introduction" in Implantable Biomedical Microsystems: Design Principles and Applications, *Elsevier Science and Technology*, MA, USA, 1st Edition, ISBN: 0323262082, February 2015.

3. Saibal Mukhopadhyay, Kaushik Roy, Hillery Hunter, and **Swarup Bhunia**, "Guest Editorial: Computing in Emerging Technologies (First Issue)", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, December 2014.
4. **Swarup Bhunia**, Leyla Nazhandali, and Dakshi Agrawal, "Guest Editors' Introduction: Trusted System with Untrusted Components: An Emerging Design Need", *IEEE Design & Test of Computers (D&T)*, April 2013.
5. Somnath Paul and **Swarup Bhunia**, "Preface" in Computing with Memory for Energy-Efficient Robust Systems, *Springer*, New York, USA, ISBN: 1461477972, September 2013.
6. **Swarup Bhunia** and Darrin J. Young, "Introduction to Special Issue on Implantable Electronics", *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Vol. 8, No. 2, pp. 7.1-7.2, June 2012.
7. **Swarup Bhunia** and Rahul Rao, "Guest Editors' Introduction: Managing Uncertainty through Postfabrication Calibration and Repair", *IEEE Design & Test of Computers (D&T)*, Vol. 27, No. 6, pp. 4-5, November 2010.
8. **Swarup Bhunia** and Saibal Mukhopadhyay, "Preface" in Low-Power Variation Tolerant Design in Nanometer Silicon, *Springer*, New York, USA, 1st Edition, ISBN: 1441974172, November 2010.
9. **Swarup Bhunia**, "A Special Issue on 23rd IEEE International Conference on VLSI Design, Bangalore, India, 3-7 January 2010", *Journal of Low Power Electronics (JOLPE)*, Vol. 6, No. 3, pp. 375-375, October 2010.

Patents and Invention Disclosures

Patents

1. Patent 8402401.US: Rajat Subhra Chakraborty, Seetharam Narasimhan and **Swarup Bhunia**, "Protection of Intellectual Property (IP) cores through a design flow", filed by Case Western Reserve University on November 9, 2010, issued on March 19, 2013. [Filed by CWRU]
2. Patent 7454738.US: **Swarup Bhunia**, Nilanjan Banerjee, Hamid Mahmoodi, Qikai Chen, and Kaushik Roy, "Synthesis Approach for Active Leakage Power Reduction Using Dynamic Supply Gating", issued November 2008.
3. Patent 7548473.US: Qikai Chen, Hamid Mahmoodi, **Swarup Bhunia** and Kaushik Roy, "Apparatus and Methods for Determining Memory Device Faults", issued June 2009.
4. Patent 7319343.US: **Swarup Bhunia**, Hamid Mahmoodi, Arijit Raychowhury, Saibal Mukhopadhyay, and Kaushik Roy, "Low Power Scan Design and Delay Fault Testing Technique Using First Level Supply Gating", issued January 2008.

Invention Disclosures

1. Xinmu Wang, Abhishek Basak, Yu Zheng, and **Swarup Bhunia**, "A Centralized and Configurable Infrastructure IP for Secure System-on-Chip Design", Case No. 2015-2732, Aug 27, 2014, Case Western Reserve University.
2. Margot Damaser, **Swarup Bhunia**, Robert Karam, Steve Majerus, Dennis Bournbeau, "Abdominal Pressure Free Bladder Contraction Detection System", Cleveland Clinic Foundation, Aug 22, 2014.
3. Fengchao Zhang, Philip Feng, Tina He, and **Swarup Bhunia**, "Silicon Carbide (SiC) Nanoelectromechanical Antifuse For Ultralow-Power Field Programmable Gate Arrays (FPGA)", Case No. 2014-261, Nov 8, 2013, Case Western Reserve University.
4. Abhishek Basak, Vasihnavi Ranganathan, and **Swarup Bhunia**, "A Wearable Ultrasonic Assembly For Point-Of-Care Autonomous Diagnostics Of Malignant Growth", Case No. 2013-2456, March 13, 2013, Case Western Reserve University.
5. Aswin Krishna, Seetharam Narasimhan, Xinmu Wang, and **Swarup Bhunia**, "Memory Based PUF Using Embedded Memory And Scan Chains", Case No. 2012-2184, Dec 2011, Case Western Reserve University.

6. Abhishek Basak, Seetharam Narasimhan, and **Swarup Bhunia**, "A Low-Power Implanted Ultrasonic Imaging Assembly For High Resolution, Online Monitoring Of Tumor Growth", August 2011, Case Western Reserve University.
7. **Swarup Bhunia**, Seetharam Narasimhan, Francis Wolff, Xinmu Wang, Anandaroop Ghosh, Hari Rajgopal, Chris Roberts, Te-Hao Li, and Mehran Mehregany, "NEMS/MEMS Multi-Layer Beam Switch and Other Custom Structures for All-Mechanical Random Logic and FPGA Design", March 2010, Case Western Reserve University.
8. Rajat Subhra Chakraborty and **Swarup Bhunia**, "Embedded Software Protection through Key-Based Control and Data Flow Obfuscation", Feb 2010, Case Western Reserve University.
9. Somnath Paul and **Swarup Bhunia**, "Reliability-Driven Variable ECC Allocation for Correction of Multiple Errors in Processor Cache", Jan 2010, Case Western Reserve University.
10. Rajat Subhra Chakraborty, Somnath Paul, Francis Wolff, Chris Papachristou and **Swarup Bhunia**, A Statistical Approach to Hardware Trojan Detection using N-Detect Tests and Coverage Estimation using Random Sampling, April 2009, Case Western Reserve University.
11. Seetharam Narasimhan, Hillel Chiel, and **Swarup Bhunia**, "Vocabulary-Based Neural Pattern Analyzer for Behaviorally Significant Burst Pattern Recognition", April 2009, Case Western Reserve University.
12. Rajat Subhra Chakraborty, Seetharam Narasimhan and **Swarup Bhunia**, "Hardware IP Protection at Different Levels of Design Abstraction", Dec 2008, Case Western Reserve University.
13. **Swarup Bhunia,** Massood Tabib-Azar, and Daniel Saab, "Computer Architectures for Complementary Nanotube Electromechanical Switches", May 2006, Case Western Reserve University.
14. Abhishek Basak, Seetharam Narasimhan, and **Swarup Bhunia**, "An Integrated Sensing System for Monitoring Kids' Health in Daycare", Oct, 2010, Case Western Reserve University.
15. Seetharam Narasimhan and **Swarup Bhunia**, "Hardware Trojan Detection Using Side-Channel Analysis: Multiple-Parameter Approach and Spatial/Temporal Self-Referencing", Nov 2010, Case Western Reserve University.
16. **Swarup Bhunia**, Leyla Nazhandali, and Dakshi Agrawal, "Guest Editors' Introduction: Trusted System with Untrusted Components: An Emerging Design Need", *IEEE Design & Test of Computers*, April 2013.
17. Somnath Paul and **Swarup Bhunia**, "Preface" in Computing with Memory for Energy-Efficient Robust Systems, *Springer*, New York, USA, ISBN-10: 1461477972, 2013.
18. **Swarup Bhunia** and Darrin J. Young, "Introduction to Special Issue on Implantable Electronics", *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Vol. 8, No. 2, pp. 7.1-7.2, June 2012.
19. **Swarup Bhunia** and Rahul Rao, "Guest Editors' Introduction: Managing Uncertainty through Postfabrication Calibration and Repair", *IEEE Design & Test of Computers*, Vol. 27, No. 6, pp. 4-5, November 2010.
20. **Swarup Bhunia** and Saibal Mukhopadhyay, "Preface" in Low-Power Variation Tolerant Design in Nanometer Silicon, *Springer*, New York, USA, 1st Edition, ISBN: 1441974172, November 2010.
21. **Swarup Bhunia**, "A Special Issue on 23rd IEEE International Conference on VLSI Design, Bangalore, India, 3-7 January 2010", *Journal of Low Power Electronics (JOLPE)*, Vol. 6, No. 3, pp. 375-375, October 2010.

Invited Talks / Panels / Tutorials

1. Presentation in *Boeing Network & Space Systems*, on Hardware IP trust and security, February 17, 2015, Via Telecon, Upcoming
2. Presentation in *Freescale Semiconductor*, on trust issues and solutions in hardware intellectual property (IP), Dec 5, 2014
3. Presentation in *Army Research Office (ARO) Workshop* at NYU-Poly, New York, on infrastructure for system-on-chip security, Nov 12-13, 2014
4. Presentation at *EDA Workshop,* on secure and trustworthy hardware, Daejeon, Korea, on August 26, 2014
5. Presentation at *Samsung Electronics* on new directions in security and energy-efficiency, Su-Won, Korea on August 26, 2014
6. Presentation at *Pohang University of Science and Technology (POSTECH)* on new directions in security and energy-efficiency, Pohang, Korea, on August 27, 2014
7. Presentation at *Korea University* on system-on-chip security, Seoul, Korea, on August 28, 2014

8. Presentation in *Hathaway Brown High School* on Cybersecurity, Shaker Heights, Cleveland, May 15, 2014
9. Presentation at *Intel University Research Office (URO) workshop* on Security Design and Verification, at Portland, OR, USA on Nov 22, 2013
10. Presentation at *Army Research Office (ARO) Workshop* at NYU-Poly, New York, on Supply Chain Risk Mitigation, Nov 12, 2013
11. Presentation to *Freescale Semiconductor*, Austin, TX, USA, on System-on-Chip (SoC) Security, Sept 12, 2013
12. Presentation to *Intel Corporation*, Portland, Microprocessor Research Lab, on memory-centric scalable co-processor (via Telecon), April 5, 2013
13. Presentation at *University of Florida*, Dept. of CISE, on Hardware Security, March 15, 2013
14. Presentation at *Texas Instruments*, Dallas (Microcontroller group) on Energy-Efficient Computing, March 13, 2013
15. Presentation at *Lockheed Martin*, Akron, OH as an guest speaker in the Engineer's Week celebration, on security of electronics, February 19, 2013
16. Presentation to *Intel Circuit Research Lab (CRL)*, Portland, OR, USA on in-memory acceleration, Nov 20, 2012 (via Telecon)
17. Presentation in *Design and Test Summer School*, Oct 25-26, 2012, Puebla, Mexico, organized by National Institute for Astrophysics, Optics, and Electronics, (INAOE), Mexico
18. Presentation in *Qualcomm Inc.*, San Diego on Adaptive Computing for Low Power and Variation Tolerance, Aug 2012
19. Presentation at *IBM TJ Watson Research Lab* (New York, USA) on nanocomputing architecture, June 2012
20. Presentation at *Indian Institute of Technology (IIT)*, Kharagpur on nanocomputing, Jan 2012
21. Presentation at *Korea University*, Seoul, Korea, on low-power and robust nanoscale architecture, Aug 2011
22. Presentation at *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2011 in special session on self-healing circuits
23. Presentation in *ARO Special Workshop on Hardware Assurance* in Washington DC, Monday, April 11, 2011
24. Presentation in *IBM Austin Research Lab (ARL)*, Austin, TX, Monday, Nov 1, 2010
25. Presentation at *Intel Corporation* workshop on external academic research, Portland, OR, USA, Sept 27, 2010
26. Presentation at *Intel Circuit Research Lab (CRL)*, on adaptive computing, Portland, OR, USA, Aug 1, 2010

27. Presentation at "*Apprentice - VTS Edition: Season 3*", Organizer/Moderator: K. S. Kim – Samsung, *IEEE VLSI Test Symposium (VTS)*, 2010
28. Presentation at *The Asia Symposium on Quality Electronic Design (ASQED)* on "Digital Signal Processing in Bio-implantable Systems: Design Challenges and Emerging Solutions", 2010
29. Presentation at *IEEE International High Level Design Validation and Test Workshop (HLDVT)* on "Hardware Trojan: Threats and Emerging Solutions", 2009
30. Presentation at *IEEE International Symposium on Nanoscale Architecture (NANOARCH) on "*Computing with Nanoscale Memory: Model and Architecture", 2009
31. Lecture series presentation at *International Test Conference (ITC) on* "Power Dissipation, Variations and Nanoscale CMOS Design: Test Challenges and Self Calibration/Self Repair Solutions", Oct 2007
32. Presentation at *Intel Corporation*, Bangalore, India, Jan, 2010
33. Presentation at *Cryptography Research Institute (CRI)*, San Francisco, CA, USA, 2009
34. Presentation at *Intel Corporation*, Portland, OR, USA, Feb 2008
35. Presentation at *LSI Logic* on efficient speed binning, Oct 2007
36. Presentation to *Intel Circuit Research Lab (CRL)*, Portland, OR, USA, Nov, 2007
37. Presentation at *Indian Institute of Technology (IIT)*, Department of Computer Sc., Kharagpur, India, 2006
38. IEEE series presentation at *Jadavpur University*, Department of Electronics & Telecommunications Eng., Kolkata, India, 2006

Panels

1. Panelist in the Panel on "Capabilities and Gaps in Systems Security", *NSF-SRC Secure, Trustworthy, Assured and Resilient Semiconductors and Systems (STARSS) Workshop*, San Jose, USA, May 2014
2. Panelist in the Panel on "Teaching Cyber-Security in STEM Curriculums: K though PhD", *7th IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)*, Washington DC, USA, May 2014
3. Panelist in the Panel on "Hackers Not Welcomed - Security Verification Issues", *14th International Workshop on Microprocessor Test and Verification (MTV)*, Austin, USA, December 2013
4. Organizer of the Panel on "What Lies in Our (Nanoelectronic) Future?", *9th IEEE/ACM International Symposium on Nanoscale Architecture (NANOARCH)*, New York, USA, July 2013
5. Panelist in the Panel on "CAD for Nanoelectronic Circuit and Architecture - Are we there yet", *6th IEEE/ACM International Symposium on Nanoscale Architecture (NANOARCH)*, June 2010
6. Panelist in the Panel on "Challenges in Hardware Trojan Modeling and Detection", *3rd IEEE Hardware Oriented Security and Trust (HOST)*, June 2010

Tutorials [Selected through a Peer-Review Process]

1. Swaroop Ghosh, Jaydeep Kulkarni, and **Swarup Bhunia**, "Embedded Memory Design for Future Technologies: Challenges, Solutions and Applications", *Design Automation and Test in Europe (DATE)*, Grenoble, France, 2015, Organizer: Swaroop Ghosh (U. of South Florida), Upcoming [**Half-Day Tutorial**]
2. Prabhat Mishra, **Swarup Bhunia** and Srivaths Ravi, "Validation and Debug of Security and Trust Issues in Embedded Systems", *28th International Conference on VLSI Design*, 2015, Organizer: Prabhat Mishra (U. of Florida), Upcoming [**Half-Day Tutorial**]
3. Patrick Schaumont, **Swarup Bhunia**, Kazuo Sakiyama, and Makoto Nagata, "Hardware Trust in VLSI Design and Implementations", Organizer: Kazuo Sakiyama (UEC) and Makoto Nagata (Kobe University), in *20th Asia South Pacific Design Automation Conference (ASPDAC)*, Tokyo, Japan, 2015, Upcoming [**Full-Day Tutorial**]
4. **Swarup Bhunia**, "Secure and Trustworthy System-on-Chip: Threats and Protections", in 16th International Symposium on Quality Electronic Design (ISQED 2015), Organizer: Arijit Raychowdhury (Georgia Tech), Upcoming [**Embedded Tutorial**]
5. **Swarup Bhunia**, "Secure and Trusted SoC: Challenges and Emerging Solutions", in *14th International Workshop on Microprocessor Test and Verification (MTV)*, Austin, USA, 2013, Special Session on Security test and verification. [**Embedded Tutorial**]
6. **Swarup Bhunia**, "The art and Science of Nanomechanical Computing", in *27th International Conference on VLSI Design (VLSI-D)*, 2014, Special Session on "Computing with Post-CMOS Technologies", Organizer: Kaushik Roy, Purdue University [**Embedded Tutorial**]
7. **Swarup Bhunia**, "Ultralow Power Computing at Extreme with Silicon Carbide Nanoelectromechanical Logic", in *Design Automation and Test in Europe (DATE)*, 2014, Special Session on "Beyond CMOS Ultra-low-power Electronics", Organizer: Saibal Mukhopadhyay, GaTech [**Hot Topic Session**]
8. **Swarup Bhunia**, "Energy-Efficient Hardware Acceleration through Computing in the Memory", in *Design Automation and Test in Europe (DATE)*, 2014, Special Session on "Memcomputing: the Cape of Good Hope", Organizer: Hung-Ming Chen, National Chiao Tung University, Taiwan & Yiyu Shi, Missouri University of Science & Technology [**Embedded Tutorial**]
9. Srivaths Ravi, Anand Ragunathan, Eric Peeters, and **Swarup Bhunia**, "Designing Secure SoCs", in 26th *IEEE International Conference on VLSI Design (VLSI-D)*, 2013. Organizer: Srivaths Ravi, Texas Instruments. [**Full-Day Tutorial**]
10. Susmita Sur-Kolay and **Swarup Bhunia**, "Intellectual Property Protection and Security in System on a Chip", in 25th *IEEE International Conference on VLSI Design (VLSI-D)*, 2012. Organizer: Susmita Sur-Kolay, Indian Statistical Institute. [**Full-Day Tutorial**]
11. Rahul Rao, Saibal Mukhopadhyay, **Swarup Bhunia**, and Praveen Elakkumanan, "*Parameter Variations and Low-Power Design: Test Issues and On-chip Calibration/Repair Solutions*", in *International Test Conference (ITC)*, 2010. Organizer: Rahul Rao, IBM Research. [**Full-Day Tutorial**]

12. Rahul Rao, Saibal Mukhopadhyay, **Swarup Bhunia**, and Praveen Elakkumanan, "*Parameter Variations and Low-Power Design: Test Issues and On-chip Calibration/Repair Solutions*", in *VLSI Test Symposium (VTS)*, 2010. Organizer: Rahul Rao, IBM Research. [**Full-Day Tutorial**]
13. Rahul Rao, Praveen Elakkumanan, Saibal Mukhopadhyay and **Swarup Bhunia**, "Parametric Failures and Self-Calibration/Self-Repair Solutions", in *International Test Conference (ITC)*, 2009. Organizer: Saibal Mukhopadhyay, Georgia Tech. [**Full-Day Tutorial**]
14. **Swarup Bhunia**, Kanak B. Agarwal and Kaushik Roy, "Low Power Design under Parameter Variations", in *Design Automation and Test in Europe (DATE) Conference*, 2009. Organizer: Swarup Bhunia, Case Western Reserve U. [**Half-Day Tutorial**]
15. Saibal Mukhopadhyay, Rahul Rao, Praveen Elakkumanan, and **Swarup Bhunia**, "Parametric Failures and Self-Calibration/Self-Repair Solutions in Nanometer Technologies", in *IEEE International On-Line Test Symposium (IOLTS), 2009*. Organizer: Saibal Mukhopadhayay, Georgia Tech. [**Full-Day Tutorial**]
16. **Swarup Bhunia**, "Variation-Tolerant Low-Power Logic Circuit", in *International Symposium on Quality Electronic Design (ISQED)*, 2009. Organizer: Rajiv Joshi, IBM Research. [**Embedded Tutorial**]
17. **Swarup Bhunia** and Kaushik Roy, "Low Power Design under Parameter Variations", in *IEEE International SOC Conference (SOCC)*, 2008. Organizer: Swarup Bhunia, Case Western Reserve U. [**Half-Day Tutorial**]
18. Kaushik Roy and **Swarup Bhunia**, "Low Power Design under Parameter Variations", in *International Symposium on Low Power Electronics and Design (ISLPED)*, 2008. Organizer: Swarup Bhunia, Case Western Reserve U. [**Embedded Tutorial**]
19. **Swarup Bhunia** and Kaushik Roy, "Process Variations and Process-Tolerant Design", in *International Conference on VLSI Design,* 2007. Organizer: Swarup Bhunia, Case Western Reserve U. [**Embedded Tutorial**]